WHAT IS CLAIMED IS:

1. A data writing method for a semiconductor memory device having a first memory cell block capable of rewriting data and having at least one first memory cell; and a second memory cell block capable of rewriting data and having at least one second memory cell adjoining said first memory cell, said method comprising:

writing data into said first memory cell;

writing data into said second memory cell following writing the data into said first memory cell;

verifying the data of said first memory cell after writing the data into said second memory cell; and

rewriting the data into said first memory cell when insufficiency of the data of said first memory cell as a result of verifying the data of said first memory cell.

2. The method according to claim 1, wherein said first and second memory cells have an charge accumulation layer, respectively, in which the electric charge is injected or discharged in association with the data to be stored and store the data of 2 values or more as an electric charge amount.

3. The method according to claim 1, wherein said first and second memory cells have an charge accumulation layer, respectively, in which the electric charge is injected or discharged in association with

the data to be stored, store the data of 2 values or more as an electric charge amount and store the data of 3 values or more supplied from the outside in association with the data of 2 values of each of said first and second memory cells.

4. A data writing method for a semiconductor memory device having a memory cell block capable of rewriting data, wherein said memory cell block has at least two first and second memory cells connected in series or in parallel and adjoin each other, said method comprising:

writing data into said first memory cell;

writing data into said second memory cell following writing the data into said first memory cell;

verifying the data of said first memory cell after writing the data into said second memory cell; and

rewriting the data into said first memory cell when insufficiency of the data of said first memory cell as a result of verifying the data of said first memory cell.

5. The method according to claim 4, wherein said first and second memory cells have an charge accumulation layer, respectively, in which the electric charge is injected or discharged in association with the data to be stored and store the data of 2 values or more as an electric charge amount.

6. The method according to claim 4, wherein said

first and second memory cells have an charge accumulation layer, respectively, in which the electric charge is injected or discharged in association with the data to be stored, store the data of 2 values or more as an electric charge amount and store the data of 3 values or more supplied from the outside in association with the data of 2 values of each of said first and second memory cells.

7. A semiconductor integrated circuit device comprising:

a first memory cell block capable of rewriting data, said first memory cell block having at least one first memory cell;

a second memory cell block capable of rewriting data, said second memory cell block having at least one second memory cell adjacent to said first memory cell;

a first data transfer line, said first data transfer line being electrically connected to said first memory cell block directly or via a selective element to select said first memory cell block;

a second data transfer line, said second data transfer line being electrically connected to said second memory cell block directly or via a selective element to select said second memory cell block;

a charge circuit, said charge circuit charging any one of said first data transfer line and said second data transfer line;

a first data store circuit, said first data store circuit having a stable point in at least two voltages;

a second data store circuit, said second data store circuit being electrically connected to said first data store circuit;

a third data store circuit, said third data store circuit being electrically connected to said first data store circuit;

a charge/discharge circuit, said charge/discharge circuit charging or discharging a first voltage node on the basis of the data held in said third data store circuit;

a first connecting circuit, said first connecting circuit electrically connecting said first voltage node to any one of said first and second data transfer lines;

a fourth data store circuit, said fourth data store circuit having a stable point in at least two voltages; and

a second connecting circuit, said second connecting circuit electrically connecting said fourth data store circuit to said first voltage node.

8. The device according to claim 7, wherein a plurality of said semiconductor integrated circuit device is arranged in a direction orthogonal to said first and second data transfer lines; and

said semiconductor integrated circuit device

further comprises:

a data input/output line which extends in a direction orthogonal to said first and second data transfer lines; and

a third connecting circuit, which electrically connects said data input/output line to said fourth data store circuit included by each of said plurality of semiconductor integrated circuit devices.

9. The device according to claim 7, wherein a plurality of said semiconductor integrated circuit device is arranged in a direction orthogonal to said first and second data transfer lines; and

said semiconductor integrated circuit device further comprises:

control lines to control said first, second, third and fourth data store circuits, and said charge/discharge circuit included in each of said plurality of said semiconductor integrated circuit device,

wherein said control lines are used in common in said plurality of semiconductor integrated circuit device.

10. The device according to claim 9, wherein the number of said first data transfer lines is two and the number of said second data transfer lines is two.

11. The device according to claim 9, wherein the number of said first data transfer lines is four and

the number of said second data transfer lines is four.

12. The device according to claim 7, wherein said first data store circuit and said fourth data store circuit are flip flops, which include two inverters, respectively.

13. The device according to claim 7, wherein the number of transistors included in said second data store circuit is less than the number of the transistors included in said first data store circuit and the number of the transistors included in said fourth data store circuit.

14. The device according to claim 7, wherein the data is written into said second memory cell after writing the data into said first memory cell, and the data is not simultaneously written into said first and second memory cells.

15. The device according to claim 7, wherein a data input terminal of said third data store circuit is electrically connected to said first data store circuit via a third connecting circuit; and

said first voltage node is electrically connected to said first data store circuit via a fourth connecting circuit.

16. The device according to claim 15, wherein said third data store circuit includes a first switching element having a control electrode and a current path;

a control electrode of said first switching

element is electrically connected to said first data store circuit via said third connecting circuit; and

one end of the current path of said first switching element is connected to said first voltage node and the other end thereof is connected to a second voltage node having at least two steady values via a second switching element.

17. The device according to claim 15, wherein said third data store circuit includes a first switching element having a control electrode and a current path;

a control electrode of said first switching element is electrically connected to said first data store circuit via said third connecting circuit; and

one end of the current path of said first switching element is connected to said first voltage node via a second switching element and the other end thereof is connected to a second voltage node having at least two steady values.

18. The device according to claim 7, wherein a data input terminal of said third data store circuit is electrically connected to a second voltage node via a third connecting circuit; and

said second voltage node is electrically connected to said first voltage node via a fourth connecting circuit and said second voltage node is electrically connected to said first data store circuit via an fifth connecting circuit.

19. The device according to claim 18, wherein said third data store circuit includes a first switching element having a control electrode and a current path;

a control electrode of said first switching element is electrically connected to said second voltage node; and

one end of the current path of said first switching element is connected to said first voltage node and the other end thereof is connected to a third voltage node having at least two steady values via a second switching element.

20. The device according to claim 18, wherein said third data store circuit includes a first switching element having a control electrode and a current path;

a control electrode of said first switching element is electrically connected to said second voltage node; and

one end of the current path of said first switching element is connected to said first voltage node via a second switching element and the other end thereof is connected to a third voltage node having at least two steady values.

21. The device according to claim 7, wherein said third data store circuit includes a first switching element having a control electrode and a current path;

a control electrode of said first switching element is electrically connected to said first data

store circuit; and

one end of the current path of said first switching element is connected to said first voltage node and the other end thereof is connected to a second voltage node having at least two steady values via a second switching element.

22. The device according to claim 7, wherein said third data store circuit includes a first switching element having a control electrode and a current path;

a control electrode of said first switching element is electrically connected to said first data store circuit; and

one end of the current path of said first switching element is connected to said first voltage node via a second switching element and the other end thereof is connected to a second voltage node having at least two steady values.

23. The device according to claim 7, wherein said first and second memory cells store data of 3 values or more as a logical value.

24. The device according to claim 7, wherein each of said first and second memory cells comprises an field effect transistor having at least one charge accumulation layer and at least one control gate.

25. The device according to claim 24, wherein each of said first and second memory cells stores digital data of 4 values or more as a logical value depending

on the magnitude of the electric charge amount accumulated in said charge accumulation layer, and the adjoining digital data is inverted each other for each bit with respect to the electric charge amount in the case that the digital data are arranged in an order of said electric charge amount.

26. The device according to claim 24, wherein said field effect transistors are formed on the same conductive type well, respectively.

27. The device according to claim 26, wherein said field effect transistor uses an FN tunneling current for the writing operation.

28. The device according to claim 24, wherein said charge accumulation layer includes silicon nitride.

29. The device according to claim 28, wherein each of said first and second memory cells include at least first and second cell transistors adjoin each other, each of said first and second cell transistor have a source electrode, a drain electrode and said charge accumulation layer, said source electrode of said first cell transistor and said drain electrode of said second cell transistor connected in series each other, and distance of said charge accumulation layer of said first cell transistor and said charge accumulation layer of said second cell transistor less than twice thickness of said charge accumulation layer.

30. The device according to claim 24, wherein said

charge accumulation layer is a floating gate electrode containing polycrystalline silicon.

31. The device according to claim 30, wherein each of said first and second memory cells include at least first and second cell transistors adjoin each other, each of said first and second cell transistor have a source electrode, a drain electrode and said charge accumulation layer, said source electrode of said first cell transistor and said drain electrode of said second cell transistor connected in series each other, and distance between said charge accumulation layer of said first cell transistor and said charge accumulation layer of said second cell transistor less than twice thickness of said charge accumulation layer.

32. The device according to claim 30, wherein an insulator is only formed between the charge accumulation layer of said first memory cell and the charge accumulation layer of said second memory cell.

33. A semiconductor integrated circuit device comprising:

a memory cell block capable of rewriting data, said memory cell block having at least two first and second memory cells connected in series or in parallel and adjoin each other;

a data transfer line, said transfer line being electrically connected to said memory cell block directly or via a selective element to select said

memory cell block;

a charge circuit, said charge circuit charging said data transfer line;

a first data store circuit, said first data store circuit having a stable point in at least two voltages;

a second data store circuit, said second data store circuit being electrically connected to said first data store circuit;

a third data store circuit, said third data store circuit being electrically connected to said first data store circuit;

a charge/discharge circuit, said charge/discharge circuit charging or discharging a first voltage node on the basis of the data held in said third data store circuit;

a first connecting circuit, said first connecting circuit electrically connecting said first voltage node to said data transfer lines;

a fourth data store circuit, said fourth data store circuit having a stable point in at least two voltages; and

a second connecting circuit, said second connecting circuit electrically connecting said fourth data store circuit to said first voltage node.

34. The device according to claim 33, wherein a plurality of said semiconductor integrated circuit device is arranged in a direction orthogonal to said

data transfer line;

said semiconductor integrated circuit device further comprises a data input/output line which extends in a direction orthogonal to said data transfer line; and

a third connecting circuit, which electrically connects said data input/output line to said fourth data store circuit included by each of said plurality of semiconductor integrated circuit devices.

35. The device according to claim 33, wherein a plurality of said semiconductor integrated circuit device is arranged in a direction orthogonal to said data transfer line; and

said semiconductor integrated circuit device further comprises:

control lines to control said first, second, third and fourth data store circuits, and said charge/discharge circuit included in each of said plurality of said semiconductor integrated circuit device,

wherein said control lines are used in common in said plurality of semiconductor integrated circuit device.

36. The device according to claim 35, wherein the number of said data transfer lines for each of said plurality of said semiconductor integrated circuit device is two.

37. The device according to claim 35, wherein the number of said first data transfer lines for each of said plurality of said semiconductor integrated circuit device is four.

38. The device according to claim 33, wherein said first data store circuit and said fourth data store circuit are flip flops, which include two inverters, respectively.

39. The device according to claim 33, wherein the number of transistors included in said second data store circuit is less than the number of the transistors included in said first data store circuit and the number of the transistors included in said fourth data store circuit.

40. The device according to claim 33, wherein the data is written into said second memory cell after writing the data into said first memory cell, and the data is not simultaneously written into said first and second memory cells.

41. The device according to claim 33, wherein a data input terminal of said third data store circuit is electrically connected to said first data store circuit via a third connecting circuit; and

said first voltage node is electrically connected to said first data store circuit via a fourth connecting circuit.

42. The device according to claim 41, wherein said

third data store circuit includes a first switching element having a control electrode and a current path;

a control electrode of said first switching element is electrically connected to said first data store circuit via said third connecting circuit; and

one end of the current path of said first switching element is connected to said first voltage node and the other end thereof is connected to a second voltage node having at least two steady values via a second switching element.

43. The device according to claim 41, wherein said third data store circuit includes a first switching element having a control electrode and a current path;

a control electrode of said first switching element is electrically connected to said first data store circuit via said third connecting circuit; and

one end of the current path of said first switching element is connected to said first voltage node via a second switching element and the other end thereof is connected to a second voltage node having at least two steady values.

44. The device according to claim 33, wherein a data input terminal of said third data store circuit is electrically connected to a second voltage node via a third connecting circuit; and

said second voltage node is electrically connected to said first voltage node via a fourth connecting

circuit and said second voltage node is electrically connected to said first data store circuit via an fifth connecting circuit.

45. The device according to claim 44, wherein said third data store circuit includes a first switching element having a control electrode and a current path;

a control electrode of said first switching element is electrically connected to said second voltage node; and

one end of the current path of said first switching element is connected to said first voltage node and the other end thereof is connected to a third voltage node having at least two steady values via a second switching element.

46. The device according to claim 44, wherein said third data store circuit includes a first switching element having a control electrode and a current path;

a control electrode of said first switching element is electrically connected to said second voltage node; and

one end of the current path of said first switching element is connected to said first voltage node via a second switching element and the other end thereof is connected to a third voltage node having at least two steady values.

47. The device according to claim 33, wherein said third data store circuit includes a first switching

element having a control electrode and a current path;

a control electrode of said first switching element is electrically connected to said first data store circuit; and

one end of the current path of said first switching element is connected to said first voltage node and the other end thereof is connected to a second voltage node having at least two steady values via a second switching element.

48. The device according to claim 33, wherein said third data store circuit includes a first switching element having a control electrode and a current path;

a control electrode of said first switching element is electrically connected to said first data store circuit; and

one end of the current path of said first switching element is connected to said first voltage node via a second switching element and the other end thereof is connected to a second voltage node having at least two steady values.

49. The device according to claim 33, wherein said first and second memory cells store data of 3 values or more as a logical value.

50. The device according to claim 33, wherein each of said first and second memory cells comprises an field effect transistor having at least one charge accumulation layer and at least one control gate.

51. The device according to claim 50, wherein each of said first and second memory cells stores digital data of 4 values or more as a logical value depending on the magnitude of the electric charge amount accumulated in said charge accumulation layer, and the adjoining digital data is inverted each other for each bit with respect to the electric charge amount in the case that the digital data are arranged in an order of said electric charge amount.

52. The device according to claim 50, wherein said field effect transistors are formed on the same conductive type well, respectively.

53. The device according to claim 52, wherein said field effect transistor uses an FN tunneling current for the writing operation.

54. The device according to claim 50, wherein said charge accumulation layer includes silicon nitride.

55. The device according to claim 54, wherein each of said first and second memory cells include at least first and second cell transistors adjoin each other, each of said first and second cell transistor have a source electrode, a drain electrode and said charge accumulation layer, said source electrode of said first cell transistor and said drain electrode of said second cell transistor connected in series each other, and distance of said charge accumulation layer of said first cell transistor and said charge accumulation

layer of said second cell transistor less than twice thickness of said charge accumulation layer.

56. The device according to claim 50, wherein said charge accumulation layer is a floating gate electrode containing polycrystalline silicon.

57. The device according to claim 56, wherein each of said first and second memory cells include at least first and second cell transistors adjoin each other, each of said first and second cell transistor have a source electrode, a drain electrode and said charge accumulation layer, said source electrode of said first cell transistor and said drain electrode of said second cell transistor connected in series each other, and distance between said charge accumulation layer of said first cell transistor and said charge accumulation layer of said second cell transistor less than twice thickness of said charge accumulation layer.

58. The device according to claim 56, wherein an insulator is only formed between the charge accumulation layer of said first memory cell and the charge accumulation layer of said second memory cell.

59. A semiconductor integrated circuit device comprising:

a first memory cell array, said first memory cell array including first and second memory cell blocks capable of rewriting data and having a plurality of memory cells, which are arranged each other in a

direction orthogonal to a data transfer line and are connected in series or in parallel, and data selection lines, which are formed in a direction orthogonal to said data transfer line and are connected in parallel in said first and second memory cell blocks; wherein a memory cell of said first memory cell array stores the data of 3 values or more as a logical value; and

a second memory cell array, said second memory cell array including third and fourth memory cell blocks capable of rewriting the data and having a plurality of memory cells, which are arranged each other in a direction orthogonal to said data transfer line with respect to said first memory cell array and are connected in series or in parallel and sharing a data selection line with the data selection line of said first memory cell array, wherein a memory cell of said second memory cell array stores the data of 2 values as a logical value.

60. The device according to claim 59, wherein the number of memory cells, which are included in said second memory cell array and are connected to one data selection line, is 2 or more; and the number thereof is less than the number of memory cells, which are included in said first memory cell array and are connected to one data selection line.

61. A semiconductor integrated circuit device comprising:

a plurality of first memory blocks capable of rewriting data; and

a plurality of second memory blocks capable of rewriting data,

wherein when the data is erased from said plurality of first memory blocks and said plurality of second memory blocks, the data is written in said plurality of first memory blocks and the data is read from said plurality of second memory blocks as keeping the erasing state, the read data of said plurality of second memory blocks is identical with the read data of said first memory blocks.